

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-30. (canceled)

31. (currently amended) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas;

forming a plurality of first electrode test pads on a peripheral area of an uppermost surface of said first metal wiring layer for carrying out a provisional yield rate test;

subjecting said wafer to said provisional yield-rate test in which it is examined by using only said first electrode test pads whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; ~~and~~

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional yield-rate test[[,]];

forming a plurality of second electrode test pads on a peripheral area of an uppermost surface of said second metal wiring layer for carrying out a genuine yield-rate test, said second electrode test pads being arranged above said first electrode test pads with at least one insulating layer being intervened therebetween;

subjecting said wafer to said genuine yield-rate test in which it is examined by using only said second electrode test pads whether each of said finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

further processing said wafer when said wafer passes said genuine yield-rate test

~~wherein a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield rate test, and it is determined that said wafer has passed said provisional yield-rate test when said yield-rate exceeds a predetermined permissible rate.~~

32. (previously presented) The production process as set forth in claim 31, wherein said first metal wiring layer is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second metal wiring layer is formed as a customized wiring-arrangement section to establish electrical

interconnections among said basic electrical component formation areas in accordance with a customer's request.

33. (currently amended) The production process as set forth in claim 31 32, wherein ~~said customized wiring arrangement section has a plurality of electrode pads formed on an uppermost surface of said second metal wiring layer, and wherein the electrode pads of said second metal wiring layer are arranged above the electrode pads of the first metal wiring layer with at least one insulating layer being intervened therebetween~~ a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provisional yield-rate test when said yield-rate exceeds a predetermined permissible rate.

34. (canceled).

35. (currently amended) The production process as set forth in claim 31 34, wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate.

36. (canceled).

37. (currently amended) The production process as set forth in claim 31 36, wherein said first metal wiring layer is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one

insulation layer alternately laminated on each of said chip areas, and said second metal wiring layer is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said first metal wiring layer.

38. (currently amended) The production process as set forth in claim 31 ~~36~~, wherein the electrode pads of the second metal wiring layer are vertically above the electrode pads of the first metal wiring layer.

39. (currently amended) A process for producing a plurality of semiconductor devices on chip areas of a wafer, said process comprising:

forming a first metal wiring layer on each of the chip areas, said first metal wiring layer having a first test section provided only at a peripheral area;

performing a provisional yield-rate test using a respective first test section to determine whether each of said first metal wiring layer is acceptable or unacceptable; and

forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional yield-rate test, said second metal wiring layer having a second test section provided vertically above said first test section; ~~that is~~ ~~different from and connected to said first metal wiring layer,~~

~~wherein said first metal wiring layer has a plurality of electrode pads formed on an uppermost surface thereof, for carrying out said provisional yield-rate test~~

performing a genuine yield-rate test using said second test section to determine whether each of said second metal wiring layer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

processing said wafer when said wafer passes said genuine yield-rate test.

40. (currently amended) The process as set forth in claim 39, ~~further comprising:~~

~~performing a genuine yield-rate test using said second test section to determine whether each of said second metal wiring layer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and~~

~~processing said wafer when said wafer passes said genuine yield-rate test~~

wherein said first metal wiring layer has a plurality of electrode pads formed on an uppermost surface of said first test section, for carrying out said provisional yield-rate test.

41. (currently amended) The process as set forth in claim 40, wherein said second metal wiring layer has a plurality of electrode pads formed on an uppermost surface of said second test section, for carrying out ~~thereof,~~ said genuine yield-rate

~~test being carried out using the electrode pads of said second metal wiring layer.~~

42. (currently amended) The process as set forth in claim 39,

wherein ~~said step of the~~ forming said first metal wiring layer comprises forming a multi-layered wiring-arrangement section comprising at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and

wherein ~~said step of the~~ forming said second metal wiring layer comprises forming a multi-layered wiring-arrangement section comprising at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said first metal wiring layer.

43. (currently amended) The ~~production~~ process as set forth in claim 39, wherein the second test section is vertically above the first test section.

44. (currently amended) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, said production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas, each said first metal wiring layer having a first test section provided

only at a peripheral area thereof and electrically connected to an active region of a respective one of said chip areas;

subjecting said wafer to a provisional yield-rate test using said first test section to determine whether each of said semi-finished semiconductor devices on said wafer is acceptable or unacceptable; ~~and~~

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional yield-rate test, each said second metal wiring layer having a second test section, ~~different than said first test section,~~ provided only in a peripheral area above said first test section and that is electrically connected to said active region of a corresponding one of said chip areas

subjecting said wafer to a genuine yield-rate test using said second test section to examine whether each of said finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

further processing said wafer when said wafer passes said genuine yield-rate test.

45. (currently amended) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming at least one first metal wiring layer on each of said chip areas, each said at least one first metal wiring layer having a first test section provided only at a peripheral area thereof;

subjecting said wafer to a provisional yield-rate test ~~in which it is examined~~ by contacting said first test section with a probe contact to determine whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable semi-finished semiconductor devices; ~~and~~

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by at least one step of depositing and patterning a metal layer to form at least one second metal wiring layer over said at least one first metal wiring layer when said wafer passes said provisional yield-rate test, each said at least one second metal wiring layer having a second test section provided above said first test section;

subjecting said wafer to a genuine yield-rate test by contacting said second test section with said probe contact to examine whether each of said finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

further processing said wafer when said wafer passes
said genuine yield-rate test.

46. (currently amended) The production process as set forth in claim 45, wherein a plurality of electrode pads are formed on an uppermost surface of said first wiring layer, for carrying out said provisional yield rate test, and wherein a plurality of electrode pads are formed on an uppermost surface of said second wiring layer, for carrying out said genuine yield-rate test.